AND8345/D

WDFN6 2x2 μCool™ 506AN Dual MOSFET Package Board Level Application Notes and Thermal Performance

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APPLICATION NOTE

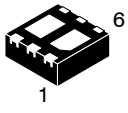
Introduction

New ON Semiconductor μCool™ MOSFETs in a WDFN6 2x2 506AN package are thermally enhanced and remarkably small to exclusively address power management challenges in portable devices such as synchronous buck and boost circuits, high and low side load switches, and lithium−ion battery charging circuits.

This technical note discusses the dual site WDFN6 506AN device package overview, pad patterns, evaluation board layout and thermal performance.

Package Overview

The WDFN6 platform offers a versatility which allows either a single or dual semiconductor device to be implemented within a leadless package. Figure 1 illustrates a dual site WDFN6 semiconductor device package and pin−out description. A half etch lead−frame complements mold lock features allowing this leadless package to provide exposed drain pads for excellent thermal conduction and reduced electrical parasitics. This low profile (< 0.8 mm) compact design is similar to the popular DFN/QFN package allowing for an easy fit in thin environments. Suggested guidelines for mounting criteria on a printed circuit board are outlined in application note AND8211/D, “Board Level Application Notes for DFN and QFN Packages”.



STYLE 1:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

Figure 1. The Underside of a Dual−Chip 6 Pin WDFN Package

Basic Pad Patterns

A recommended solder−mask defined mounting footprint is defined in Figure 2. μCool™ MOSFET 2 mm x 2 mm footprint dimensions are the same as a standard SC−88 and SC−70−6 package. However, the underside of this WDFN6 package offers an added feature of exposed flags acting as drain contacts and heat dissipation paths to promote operation at a lower junction temperature. This correlation is further explained in the thermal response section.

Figure 3 depicts a minimum recommended pad pattern that confines an improved thermal area of drain connections (pins 3, 6) to the basic footprint. Increased drain copper areas assist in directing the power dissipation path through the copper lead−frame and into the board. The addition of vias to other board layers further enhances device performance. An evaluation board containing the minimum recom−mended pad pattern and aforementioned vias is shown in Figure 4 of the subsequent section.

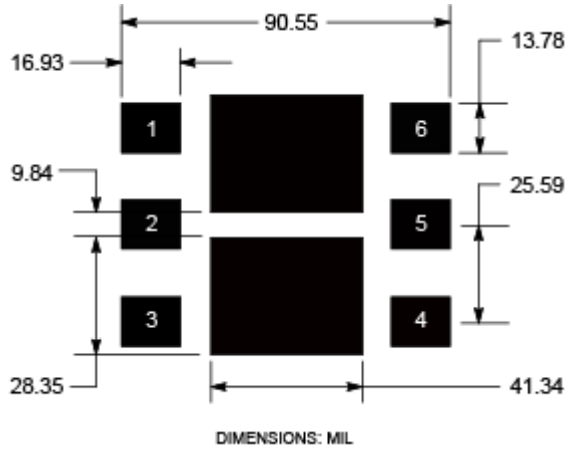


Figure 2. Basic Pad Layout

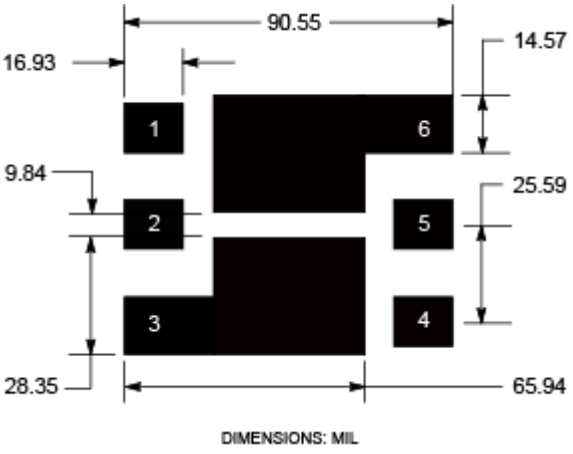
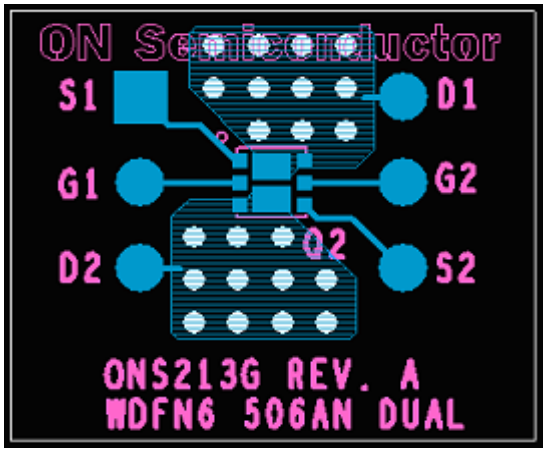


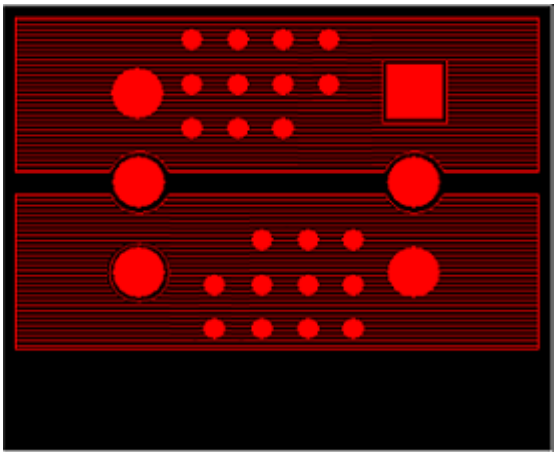
Figure 3. Minimum Recommended Pad Pattern

Evaluation Board

The evaluation board, shown in Figure 4, measures 0.6 x 0.5 inch. The board contains 1 oz copper thickness on top−side and 1 oz copper thickness on the underside. Vias are added through to the underside of the board where contact is made with a copper pad area of approximately 0.198 square inch. On top−side, the copper pad areas surrounding the two drain leads are each increased to approximately 0.034 square inch.



Front of Board



Back of Board

Figure 4. Evaluation Board

This 6−pin DIP design allows the use of sockets to assist in testing. Figure 5 represents a WDFN6 506AN package mounted on the evaluation board with and without test sockets. A quick thermal analysis of this board is conducted by inducing a saturation current in Q1 while keeping Q2 off. The saturation current of 815 mA is induced by using a 5 Ω source−load, shorting gate to source and holding the drain potential at a constant 5.082 V. This delivers an approximate 4.1 W to Q1 which yields a junction temperature of 85.4°C and a board temperature of 52.8°C. Figure 6 shows a thermal image of this board under the aforementioned conditions.

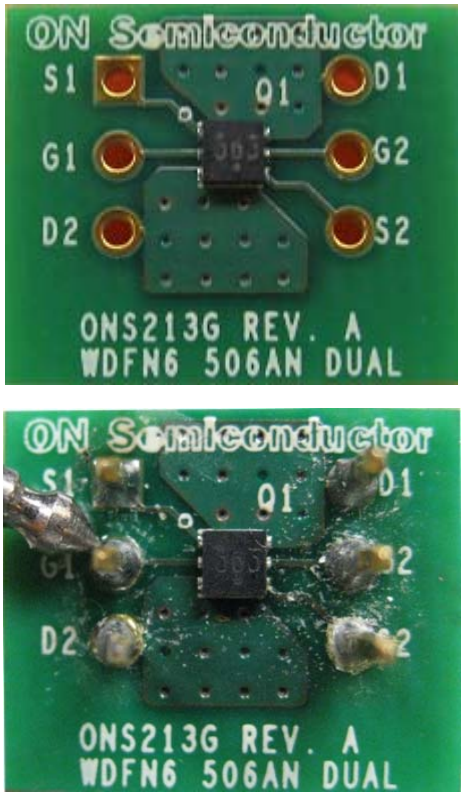


Figure 5. Mounted Device

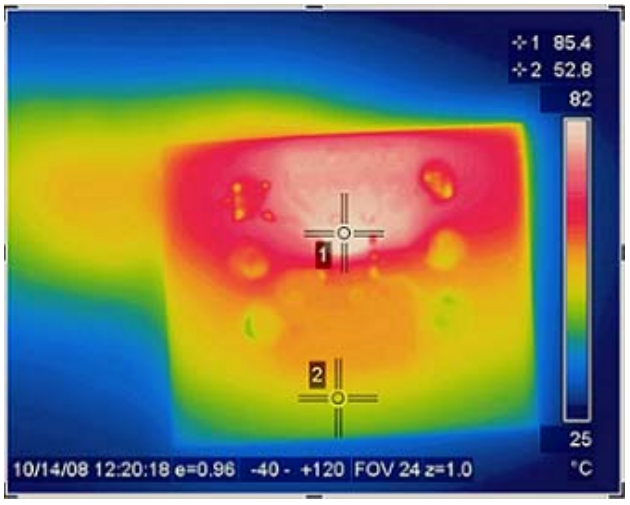


Figure 6. Thermal Image of Mounted Device

Further results from the measured thermal performance of this package are described in the subsequent section. Testing included a thermal analysis of the package surface mounted on a FR4 board using one−inch square pad size and the minimum recommended pad size.

Thermal Performance

Assumptions and Definitions

The subsequent sections outline the thermal performance of a WDFN6 506AN package. All values and equations are obtained from simulations and pertain to the Theta(DC) matrix with both MOSFETs operating at maximum power unless otherwise specified. A 10% duty cycle is arbitrarily chosen to evaluate various thermal responses. Refer to Figure 11 for thermal responses at varying duty cycles. The simulation models used to derive the results in this section are modeled around results obtained from physical testing and are considered reliable. Table 1 defines a set of parameters used throughout this section.

Table 1. Thermal Analysis Parameters

Symbol	Definition
T_{Jn}	Junction Temperature of MOSFET “n”
T_{AMB}	Ambient Temperature
P_{Dn}	Power Dissipation of MOSFET “n”
P_{TOTAL}	Total Power Dissipation
$R_{\theta-JnL}$	Thermal Resistance from Junction “n” to Location “L”
$R(u)_{EFF}$	Effective (maximum) Thermal Resistance of Package
Ψ_{QXQY}	Thermal Resistance of FET “x” due to FET “y”
Ψ_{Fn-L}	Thermal Reference between Foot “n” and location “L”
Ψ_{Jn-L}	Thermal Reference between Junction “n” and location “L”

The number designation associated with “foot” in the subscript of each Ψ (read psi) term corresponds to the pin identification number as shown in Figure 7.

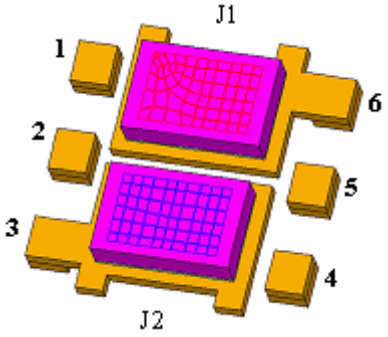


Figure 7. Foot and Junction Identification

Figures 8 and 9 represent Cauer and Foster Ladders respectively. This technical note assumes the reader has a general understanding of these networks. Please refer to the documentation cited under references for detailed descriptions of thermal RC networks. In this section, the Foster network is used to calculate various thermal characteristics. For example, as seen in Figure 9, a particular thermal resistance occurs between junction “n” and some location “L” (denoted here as Ψ_{Jn-L}). Let the thermal resistance, at the C1/C2 node, be measured from Junction “n” to foot “n”. Then, that resistance is called a junction−to−foot thermal *reference* (Ψ_{Jn-Fn}). Therefore, in the case of junction−to−C2/C3 node, the junction−to−ambient thermal *resistance* ($R_{\theta-JnA}$) is measured as the sum of thermal references such that,

$$R_{\theta-JnA} = \Psi_{Jn-Fn} + \Psi_{Fn-A} \qquad \text{(eq. 1)}$$

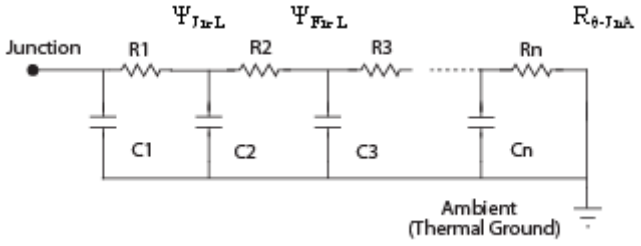


Figure 8. Grounded Capacitor Thermal Network (“Cauer” Ladder)

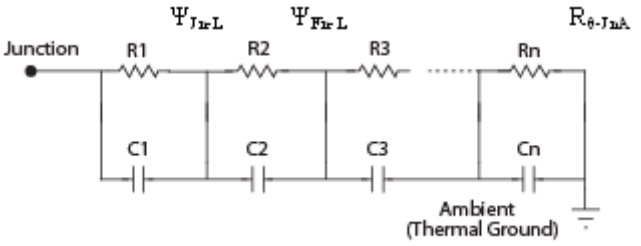


Figure 9. Non−Grounded Capacitor Thermal Network (“Foster” Ladder)

Junction−to−Foot / Foot−to−Ambient

The Foster Network junction−to−foot thermal references and foot−to−ambient thermal references are outlined in Table 2.

Table 2. Thermal Reference Parameters

	Junction−to−Foot	
10% Duty Cycle	Min−pad Size	1 in sq. Pad
Copper Area	30 mm^2 [2 oz]	1.127 in^2 [2 oz]
Ψ_{J1-F2}	30.2 °C/W	27.8 °C/W
Ψ_{J1-F3}	94.7 °C/W	69.3 °C/W
	Foot−to−Ambient	
10% Duty Cycle	**Min−pad Size**	**1 in sq. Pad**
Copper Area	30 mm^2 [2 oz]	1.127 in^2 [2 oz]
Ψ_{F2-A}	209.7 °C/W	80.4 °C/W
Ψ_{F3-A}	145.2 °C/W	38.9 °C/W

A relationship for the thermal resistance ($R_{\theta-JnA}$) of each device is established by using either of the following relationships,

$$R_{\theta-J1A} = \Psi_{J1-F2} + \Psi_{F2-A} \quad \text{(eq. 2)}$$

$$R_{\theta-J1A} = \Psi_{J1-F3} + \Psi_{F3-A} \quad \text{(eq. 3)}$$

Substituting appropriate values, from Table 2, into the above equations yields $R_{\theta-J1A} = R_{\theta-J2A} = 108.2$°C/W for the one−inch square pad size and $R_{\theta-J1A} = R_{\theta-J2A} = 239.9$°C/W for min pad size. In both cases the thermal resistances of each device are directly proportional to each other due to symmetrical die sizes.

Junction−to−Ambient

The thermal response of this package is parameterized by thermal interactions between adjacent MOSFETS. Switching one device OFF, such as Q1, alters the junction temperature and thermal resistance of each FET. Heat from Q2 will transfer to Q1 causing Q1 to exhibit an added thermal resistance equivalent to a factor of $\Psi_{Q1Q2.}$ The following matrix equation illustrates the aforementioned relationships for a junction−to−ambient thermal response;

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta-J1A} & \Psi_{Q1Q2} \\ \Psi_{Q2Q1} & R_{\theta-J2A} \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_{AMB} \quad \text{(eq. 4)}$$

Using data from Table 3, this matrix allows various junction temperatures and, in turn, the package $R(u)_{EFF}$ to be calculated at assumed ambient temperatures. $R(u)_{EFF}$ is defined as,

$$R(u)_{EFF} = \left[T_{MAX} - T_{AMB}\right] / P_{TOTAL} \quad \text{(eq. 5)}$$

Where $R(u)_{EFF}$ is a function of either direct current or a transient response and T_{MAX} is the maximum junction temperature between T_{J1} and T_{J2}. Table 3 outlines the junction−to−ambient thermal analysis of the WDFN6 506AN package surface mounted on an FR4 board. Notice that $R_{\theta-J1A} = R_{\theta-J2A}$ and $\Psi_{Q1Q2} = \Psi_{Q2Q1}$ due to symmetrical die sizes. Furthermore, Quick reference steady state matrices are located in the Appendix.

Note: * *Refer to the Appendix for Theta(t) matrix equations.*

Table 3. Junction−to−Ambient Thermal Response

	Steady State		Pulsed Time = 5 seconds
10% Duty Cycle	1 in sq. Pad	Min−pad Size	1 in sq. Pad
Copper area	1.127 in^2 [2 oz]	30 mm^2 [2 oz]	1.127 in^2 [2 oz]
$P_{D1} = P_{D2}$	1.50 W	0.71 W	2.3 W
T_{AMB}	25.0°C	25.0°C	25.0°C
$R_{\theta-J1A} = R_{\theta-J2A}$	108.21°C/W	239.94°C/W	108.21°C/W*
$\Psi_{Q1Q2} = \Psi_{Q2Q1}$	51.85°C/W	158.8°C/W	51.85°C/W*
T_{J1}	265.1°C	308.1°C	393.1°C*
T_{J2}			
T_J (single pulse)			228.4°C
T_J (pulsed)			244.8°C
$R(DC)_{EFF}$	80.0°C/W	199.4°C/W	80.0°C/W
$R(t)_{EFF}$			44.2°C/W*

Junction−to−Board

A matrix equation defining junction temperatures for assumed board temperatures is defined by Equation 6.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} \Psi_{J1-F2} & (\Psi_{Q1Q2} - \Psi_{F3-A}) \\ (\Psi_{Q2Q1} - \Psi_{F3-A}) & \Psi_{J1-F2} \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_{BOARD} \quad \text{(eq. 6)}$$

Data from Table 2 and Table 3 can be used with Equation 6 to calculate various junction temperatures at assumed board temperatures. Table 4 outlines the junction-to-board thermal analysis of a WDFN6 506AN package surface mounted on an FR4 board. Furthermore, Quick reference steady state matrices are located in the Appendix.

Table 4. Junction−to−Board Thermal Response

10% Duty Cycle	Steady State		Pulsed Time = 5 seconds
	1 in sq. Pad	Min−pad Size	1 in sq. Pad
Cu area	1.127 in^2 [2 oz]	30 mm^2 [2 oz]	1.127 in^2 [2 oz]
$P_{D1} = P_{D2}$	1.50 W	0.71 W	1.50 W
T_{AMB}	25.0°C	25.0°C	25.0°C
T_{BOARD} (DC)	204.0°C	277.0°C	204.0°C
T_{BOARD} (t)*	223.4°C	286.7°C	138.3°C
T_J (single pulse)	265.1°C	308.1°C	157.6°C
T_J (pulsed)			168.4°C
$R(DC)_{EFF(BOARD)}$	59.7°C/W	177.5°C/W	59.7°C/W
$R(t)_{EFF(BOARD)}$*	66.1°C/W	184.3°C/W	37.8°C/W

Summary

Figure 10 illustrates a steady state plot of the change in thermal resistance and max power dissipation that occurs with a change in the amount of copper spread across a given area. Evaluating the plots at the minimum recommended pad size and one−inch square pad size yields the following maximum values;

Table 5. Maximum Ratings from Figure 10

10% Duty Cycle	Min−pad Size		1 in sq. Pad	
Cu area	30 mm^2 [1 oz]	30 mm^2 [2 oz]	1.127 in^2 [1 oz]	1.127 in^2 [2 oz]
$R_{\theta-J1A}$	279.1°C/W	239.9°C/W	132.7°C/W	108.2°C/W
Max Power	0.448 W	0.521 W	0.942 W	1.16 W

Figure 11 illustrates the packages change in effective thermal resistance with respect to pulse time. The plot reflects data sampled at a minimum recommended pad size (2 oz. Cu). Under steady state conditions the plot yields $R(t)_{EFF}$ = 199.38°C/W. Maintaining steady state conditions and increasing the copper area to 1.0 square inch, 2 oz Cu, will yield $R(t)_{EFF}$ = 79.99°C/W. These results show that this package exhibits more efficient thermal characteristics than the aforementioned SC−88 package. Although a SC−88 package carries the same footprint dimensions as a WDFN6 506AN, the minimum recommended pad size plot evaluated under steady state conditions yields $R(t)_{EFF}$ = 328.0°C/W. The decreased thermal resistance of a WDFN6 506AN package is attributed to the exposed flags acting as drain contacts and heat dissipation paths.

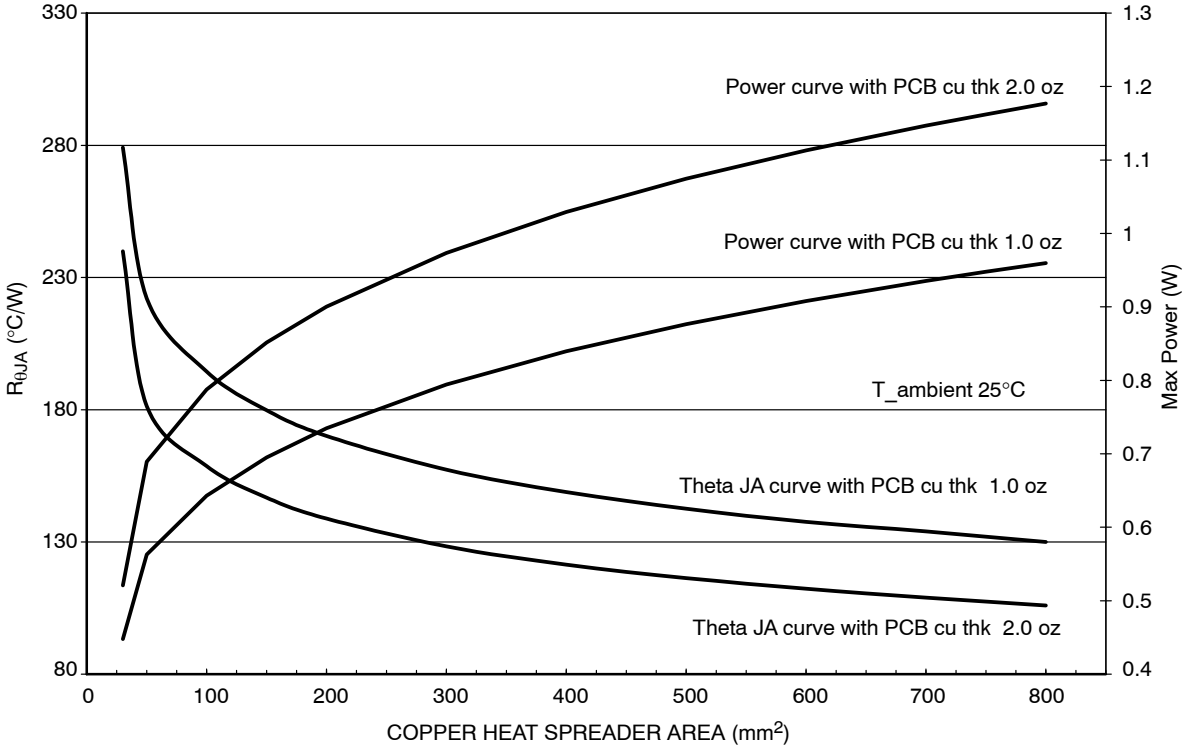


Figure 10. Self Heating Thermal Characteristics as a Function of Copper Area on the PCB

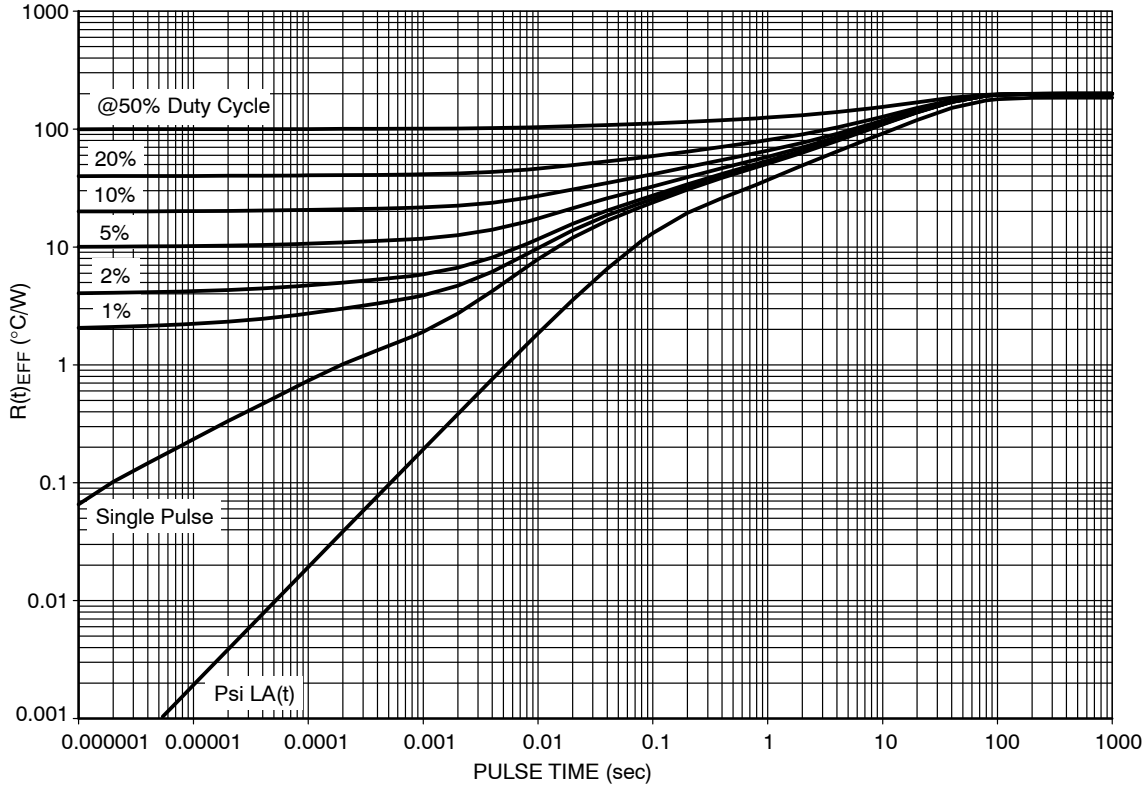


Figure 11. Thermal Response Minimum Pad Size

REFERENCES

1. R.P. Stout, D.T. Billings, “How to Extend a Thermal−RC−Network Model (Derived From Experimental Data) to Respond to an Arbitrarily Fast Input,” *On Semiconductor*, 2006.
2. R.P. Stout, “Thermal RC Ladder Networks; Packaging Technology Development,” *On Semiconductor*, 2006.
3. R.P. Stout, “General Thermal Transient RC Networks,” *On Semiconductor*, 2006.

APPENDIX

Steady State Junction−to−Ambient Quick Reference Matrix (2 oz. Cu), 10% DC

Min Pad Size

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 239.94 & 158.82 \\ 158.82 & 239.94 \end{bmatrix} \begin{Bmatrix} 0.71 \\ 0.71 \end{Bmatrix} + T_{AMB}$$

One−inch Square Pad

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 108.21 & 51.85 \\ 51.85 & 108.21 \end{bmatrix} \begin{Bmatrix} 1.5 \\ 1.5 \end{Bmatrix} + T_{AMB}$$

Junction−to−Ambient Theta(t) Matrix Equations

$$\Psi'_{QXQY} = \sum_{n=1}^{m} \Psi(\tau_n)_{J-A} \times [1 - \exp(-t_{pulse}/\tau_n)] \quad \text{(eq. 7)}$$

$$R'_{\theta-J1A} = \sum_{n=1}^{m} R(\tau_n)_{\theta-J1A} \times [1 - \exp(-t_{pulse}/\tau_n)] \quad \text{(eq. 8)}$$

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R'_{\theta-J1A} & \Psi'_{Q1Q2} \\ \Psi'_{Q2Q1} & R'_{\theta-J2A} \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_{AMB} \quad \text{(eq. 9)}$$

Steady State Junction−to−Board Quick Reference Matrix (2 oz. Cu), 10% DC.

Min Pad Size

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 209.7 & 145.24 \\ 145.24 & 209.7 \end{bmatrix} \begin{Bmatrix} 0.71 \\ 0.71 \end{Bmatrix} + T_{BOARD}$$

One−inch square Pad

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 80.4 & 38.91 \\ 38.91 & 80.4 \end{bmatrix} \begin{Bmatrix} 1.5 \\ 1.5 \end{Bmatrix} + T_{BOARD}$$

Junction−to−Board Theta(t) Matrix Equations

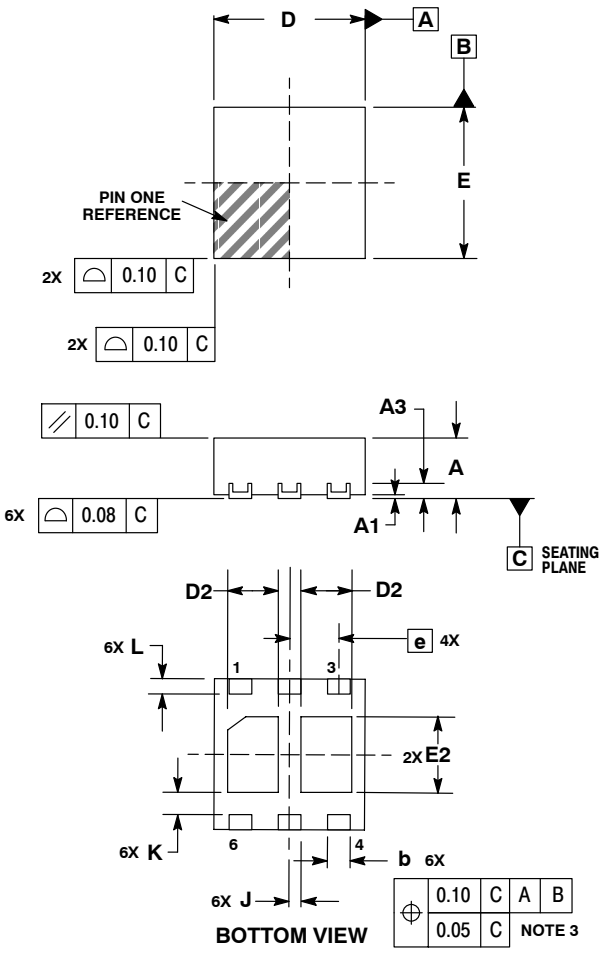
$$\Psi'_{QXQY} = \sum_{n=1}^{m} \Psi(\tau_n)_{J-A} \times [1 - \exp(-t_{pulse}/\tau_n)] \quad \text{(eq. 10)}$$

$$R'_{\theta-J1A} = \sum_{n=1}^{m} \Psi(\tau_n)_{F2-A} \times [1 - \exp(-t_{pulse}/\tau_n)] \quad \text{(eq. 11)}$$

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R'_{\theta-J1A} & \Psi'_{Q1Q2} \\ \Psi'_{Q2Q1} & R'_{\theta-J2A} \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_{BOARD} \quad \text{(eq. 12)}$$

PACKAGE DIMENSIONS

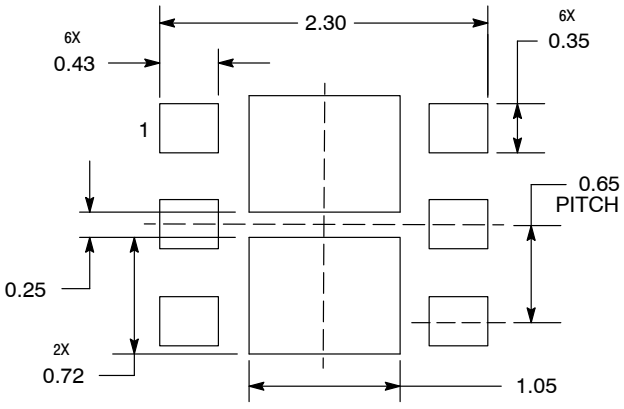
WDFN6 2x2
CASE 506AN−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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